

Applicant: T. Yanagi, et al.  
U.S.S.N.: 10/037,804  
RESPONSE TO OFFICE ACTION  
Page 11 of 19

### **REMARKS**

Applicants appreciate the Examiner's thorough examination of the subject application and request reconsideration of the subject application based on the foregoing amendments and the following remarks.

Claims 4, 5, 7, 8, 13-16, 19 and 21-28 are pending in the subject application. The Examiner acknowledges claims 13-16 as being allowable.

Claims 4, 5, 7, 19 and 21-28 stand rejected under 35 U.S.C. §102. It also was indicated that if claim 26 should be found allowable then claim 27 would be objected to under 37 C.F.R. §1.75 as being a substantial duplicate thereof. Claim 8 was objected to as depending from a rejected base claim, however, the Examiner indicated that the claim would be allowable if appropriately re-written in independent form.

Claim 27 was amended so as to provide that the slope(s) falls part of the way from High to Low. Claims 29-30 were added to more distinctly claim embodiments and/ or aspects of the present invention. The amendments to the claims are supported by the originally filed disclosure.

### **35 U.S.C. §102 REJECTIONS**

The Examiner rejected claims 4-5, 7, 19, 21-28 under 35 U.S.C. §102(e) as being anticipated by Lee et al. [US Publication 2001/ 0033266; "Lee"]. Applicants respectfully traverse as discussed below. Because claims were amended in the instant amendment, the following discussion refers to the language of the amended claims, however, only those amended

Applicant: T. Yanagi, et al.  
U.S.S.N.: 10/037,804  
RESPONSE TO OFFICE ACTION  
Page 12 of 19

features specifically relied upon to distinguish the claimed invention from the cited prior art shall be considered as being made to overcome the cited reference.

Applicants first note, however, that the cited reference, Lee, is not a proper prior art reference under 35 U.S.C. §102(e) as discussed below. The subject application claims priority to Japanese Patent Application No. 10-81994 having a filing date of March 27, 1998. Whereas the cited US published application to Lee was published On October 25, 2001 and has a filing date in the USPTO of December 14, 1998.

The certified copy of the priority document also was filed in the parent application U.S.S.N. 09/275,063, filed March 23, 1999, to which the subject divisional application also claims the benefit of domestic priority. As such, the subject divisional application has an effective earlier filing date (March 27, 1998) than the US filing date of the cited reference.

Further, Lee asserts a relation to a Japanese application that was filed in Japan on September 19, 1998. Since this filing date of the asserted related Japanese application is later in time than the effective filing date of the subject divisional application (i.e., March 27, 1998), any assertions in Lee with regards to the description of the prior art also are necessarily later in time than the earlier effective filing date of the subject application.

Notwithstanding the foregoing and in the interests of advancing prosecution, Applicants make the following additional observations or remarks. The inventions of claims 4 and 9 are directed to a display device and a display method, respectively, in which the driving circuit controls the slopes of the falls of the scanning signal based on gate voltage-drain currency characteristics of the thin film transistors.

In the thin film transistor, the drain current (ON resistance) is dependent on a gate voltage and linearly varies when a voltage in a range from the threshold voltage to the ON voltage is applied to the gate. That is, the ON state of the thin film transistor is not a binary state but is an intermediate state (the drain current varies in an analog manner in response to a gate voltage).

As is provided in the subject application (see page 19, line 13 - page 20, line 6 of the subject application):

In this case, if the falls of the scanning signal are abrupt as in the conventional cases, level shifts of the pixel potentials caused by the parasitic capacitances occur as described above, irrelevant to the gate voltage-drain current characteristic of the TFT. In the present invention [embodiment], however, it is possible to control slopes of falls of the scanning signal so that the slopes are affected when the TFT is in the state of the foregoing linear variation (intermediate ON state). Since such control causes the fall of the scanning signal to become sloped while the TFT also linearly shifts from the ON state to the OFF state in accordance with the voltage-current characteristic, each level shift of the pixel potential stemming from the parasitic capacitance is surely reduced.

The subject application also provides (see page 20, line 7 - page 22, line 11 of the subject application):

It is more preferable in the present invention to control the slopes of the falls of the scanning signal on the basis of both the signal delay transmission and the gate voltage-drain current characteristic of the TFT... In this way, it is possible not only to cancel differences in the level shifts caused by parasitic capacitances throughout the display plane, but also to reduce each level shift per se caused by the parasitic capacitance cgd... Accordingly, by applying the conventional scheme of biasing the counter potential VCOM of the counter electrode so that the level

shifts  $\Delta V_d$  stemming from the parasitic capacitances are preliminarily reduced, it is possible to provide a display device featuring lower bias level, less flickering and display defects such as burn-in residual images, and less power consumption.

The subject application also provides (see Page 23, line 21- page 24, line 3), also with reference to Fig. 3 thereof, that the slew-rate [through-rate] control elements SC (slope control sections), capable of controlling fall rates of output signals (gate-off voltages  $V_{gl}$ ), are added to the output stage of the conventional gate driver. With this arrangement, fall slopes of the scanning signals respectively outputted to the scanning signal lines can be controlled.

Lee discloses an active matrix liquid crystal display device in which “a high level gate voltage is supplied to the level shifter of the gate driver in the alternating current shave,, thereby changing the falling edge of the scanning signal into any one of the linear, exponential or ramp function shape.” Lee further asserts that the active matrix liquid crystal display device of that invention is capable of suppressing the feed through voltage  $\Delta V_p$  sufficiently as well as preventing an occurrence of flickering and residual images. Lee further discloses that, in the active matrix liquid crystal display device according to the present invention, the falling edge of the high level gate voltage has a slower slope than the rising edge thereof, thereby changing the falling edge of the scanning signal to be applied to the gate line more slowly than the rising edge thereof. Accordingly, Lee asserts that the active matrix liquid crystal display device according to that invention is capable of preventing an occurrence of a flicker and a residual image as well as providing a rapid response speed. See Lee para. 0051-052 thereof.

The present invention, in particular the inventions set forth in claim 4 and 9 of the present

invention was made in view of the problem that “the conventional scheme of biasing the counter potential VCOM of the counter electrode so that the level shifts  $\Delta V_d$  stemming from the parasitic capacitances are preliminarily reduced, is incapable of absorbing differences in the level shifts throughout the display plane, thereby being incapable of conducting optimal alternating current drive with respect to each pixel.” Accordingly, “an object of the present invention is to provide a display device which is capable of sufficiently suppressing occurrence of flickering and the like which ensue to fluctuations of pixel potentials caused by parasitic capacitances, and which is high-definition and high-performance.” See page 10, line 21 - page 11, line 15 of the subject application. In the invention as set forth in claims 4 and 19 the driving circuit controls the slopes of the falls of the scanning signal based on gate voltage-drain current characteristics of the thin film transistors to achieve this object.

In the invention disclosed in Lee, the reference suppresses the feed through voltage  $\Delta V_p$  (corresponds to the level shifts  $\Delta V_d$  of the present invention) sufficiently and prevents an occurrence of flickering and residual images as well. However, the claimed invention of claim 4 (19) and the invention disclosed in Lee differ in the driving method. That is, while Lee achieves the foregoing object by supplying a high level gate voltage to the level shifter of the gate driver in the alternating current shape, so as to change the falling edge of the high level gate voltage to be applied to the gate line more slowly than the rising edge thereof, the invention of claims 4 and 19 of the present invention achieves the object by the arrangement in which the driving circuit controls the slopes of the falls of the scanning signal based on gate voltage-drain current characteristics of said thin film transistors.

It is respectfully submitted that the foregoing remarks also apply to distinguish the other independent claims of subject application.

Claim 5 includes the further limitation that the falls of the scanning signal are sloped in an ON region of said thin film transistors. In contrast to the present invention, Lee merely describes that it has been suggested that a liquid crystal display device adopt a scanning signal control system for allowing the falling edge of the scanning signal to have a gentle slope as an alternative for suppressing the feed through voltage. While Lee provides a number of possible shapes of the waveform, Lee does not describes anywhere any particular criteria on which such shapes are or should be based. It necessarily follows that Lee does not and cannot disclose or suggest configuring and arranging the driving circuit such that the slopes of the falls of the scanning signal are based on gate voltage-drain current characteristics of the thin film transistors in an ON region of the thin-film transistors.

It also is respectfully submitted that Lee also does not teach nor suggest the particular form of the driving circuit as claimed by Applicants. In addition, it is respectfully submitted that Lee does not teach, suggest nor offer any motivation for modifying the driving circuit disclosed in the cited reference so as to yield a display device as claimed by Applicants. This is not surprising as such a modification would alter the intended operation, structure and function of the display device comprising the invention described in Lee.

As provided in MPEP-2131, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.

*Verdegal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Or

stated another way, "The identical invention must be shown in as complete detail as is contained in the ... claims. *Richardson v Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ 2d. 1913, 1920 (Fed. Cir. 1989). Although identify of terminology is not required, the elements must be arranged as required by the claim. *In re Bond*, 15 USPQ2d 1566 (Fed. Cir. 1990). It is clear from the foregoing remarks that the above-identified claims are not anticipated by the cited reference.

It is respectfully submitted that for the foregoing reasons, claims 4, 7, 19, 22-23, 26 and 27 are patentable over the cited reference and thus satisfy the requirements of 35 U.S.C. §102(e). As such, these claims, including the claims dependent therefrom are allowable.

#### CLAIM 8

In the above-referenced Office Action, claim 8 was objected to as being dependent upon a rejected base claim. It also was provided in the above-referenced Office Action, however, that the claim would be allowable if rewritten in independent form to include all the limitations of the base claim and any intervening claim(s).

As Applicants believe that the base claim is in allowable form, claim 8 was not re-written in independent form as suggested by the Examiner. However, Applicants reserve the right to later amend claim 8 so as to be in independent form.

#### CLAIM 27

In the above-referenced Office Action, Applicant was advised that if claim 26 was found to be allowable then claim 27 would be objected to under 37 C.F.R. §1.75 as being a substantial

Applicant: T. Yanagi, et al.  
U.S.S.N.: 10/037,804  
RESPONSE TO OFFICE ACTION  
Page 18 of 19

duplicate thereof.

As indicated above, claim 27 was amended in the foregoing amendment to address this objection. As such, as-amended claim 27 is considered to overcome the identified grounds of the provisional objection.

#### CLAIMS 29-30

As indicated above, claims 29-30 were added to more distinctly claim embodiments and/or aspects of the present invention. These claims are clearly supported by the originally filed disclosure, including the originally filed claims (e.g., see pages 17-22 of the subject application). It also is respectfully submitted that these added claims are patentable over the cited prior art on which the above-described rejection(s) are based.

It is respectfully submitted that the subject application is in a condition for allowance. Early and favorable action is requested.

Although claims are added, additional fees are not believed to be required. However, if



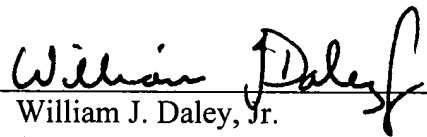
Applicant: T. Yanagi, et al.  
U.S.S.N.: 10/037,804  
RESPONSE TO OFFICE ACTION  
Page 19 of 19

for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid,  
the Commissioner is hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,  
Edwards & Angell, LLP

Date: October 17, 2003

By:



William J. Daley, Jr.  
(Reg. No. 35,487)  
P.O. Box 9169  
Boston, MA 02209  
(617) 439- 4444